What is claimed is:

1. A method of filling gaps in the plane of and between the pattern of a wiring structure on a semiconductor substrate, comprising the steps of:

Depositing a first layer of dielectric over said wiring structure thereby including the exposed surface of said semiconductor substrate;

Performing an etch back of said first layer of dielectric;

Depositing a second layer of dielectric over said etched back first layer of dielectric;

Etching said second layer of dielectric; and

Depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric.

2. The method of claim 1 wherein said wiring structure contains polysilicon.

3. The method of claim 1 wherein said wiring structure contains a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said wiring structure to be applied during the SAC process.

4. The method of claim 1 wherein said wiring structure contains an electrically conducting material.

5. The method of claim 1 wherein said first layer of dielectric contains High Density Plasma-oxide.

6. The method of claim 1 wherein said etch back of said first layer of dielectric is performing a Buffered Oxide Etch said etch back to be performed on said first layer of dielectric thereby forming a layer of first dielectric on the bottom of the holes within said wiring structure thereby further forming deposits of said first dielectric said deposits partially overlaying the top surfaces of said wiring structure.

7. The method of claim 6 wherein said BOE has a BOE solution of 10:1 or 50:1.

8. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of silicon nitride ($Si_3N_4$) said deposition covering the surface of said layer of first dielectric on the bottom of said holes within said wiring structure thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said

wiring structure thereby furthermore covering the surface of the partially exposed top corners of said wiring structure.

9. The method of claim 1 wherein said depositing said second layer of dielectric is depositing a layer of $Si_3N_4$ using PE-CVD technology at a temperature of about 400 degrees C. said layer to be deposited to a thickness between about 1000 and 2000 Angstrom.

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10. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide ($Al_3O_3$) said deposition covering the surface of said layer of first dielectric on the bottom of said holes within said wiring structure thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said wiring structure thereby furthermore covering the surface of the partially exposed top corners of said wiring structure.

11. The method of claim 1 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material having a high dielectric constant said deposition covering the surface of said layer of first dielectric on the bottom of the holes within said wiring structure thereby further covering the surface of said first dielectric

partially overlaying the top surfaces of said wiring structure thereby furthermore covering surface of the partially exposed top corners of said wiring structure.

12. The method of claim 1 wherein said etching said second layer of dielectric removing said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said wiring structure.

13. The method of claim 1 wherein said etching second layer of dielectric is etching $Si_3N_4$ using $CHF_3$ as etchant gas at a flow rate of about 15 sccm and a gas pressure of about 50 mTorr with an rf power density of about 700 watts with no magnetic field applied and an ambient wafer temperature of about 15 degrees C.

14.The method of claim 1 wherein said depositing a layer of oxide is depositing a layer of PE-oxide or PE-TEOS (Plasma Enhanced tetraethosiloxane) over said spacers on said sidewalls of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes within said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the

top surfaces of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said wiring structure.

15. The method of claim 1 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with a high dielectric constant Intra-Layer Dielectric.

16. A method of filling gaps in the plane of and between the pattern of a wiring structure on a semiconductor substrate, comprising the steps of:

Depositing a first layer of dielectric over said wiring structure thereby including the exposed surface of said semiconductor substrate;

Performing an etch back of said a first layer of dielectric wherein said etch back is performing a Buffered Oxide Etch thereby forming a layer of first dielectric on the bottom of said holes within said wiring structure thereby further forming deposits of said first dielectric on the top surfaces

of said wiring structure said deposits partially overlaying the top surfaces of said wiring structure;

Depositing a second layer of dielectric said deposition covering said layer of first dielectric on the bottom of said holes within said wiring structure thereby further covering said first dielectric partially overlaying the top surfaces of said wiring structure thereby furthermore covering the partially exposed top corners of said wiring structure;

Etching said second layer of dielectric to remove said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said wiring structure;

Depositing a layer of PE-oxide or PE-TEOS over said spacers on the sidewalls of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes within said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said wiring structure thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said wiring structure.

17. The method of claim 16 wherein said wiring structure contains polysilicon.

18. The method of claim 16 wherein said wiring structure contains a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said wiring structure to be applied during the SAC process.

19. The method of claim 16 wherein said wiring structure contains an electrically conducting material.

20. The method of claim 16 wherein said first layer of dielectric contains High Density Plasma-oxide.

21. The method of claim 16 wherein said etch back of said first layer of dielectric is a Buffered Oxide Etch (BOE) with a BOE solution of 10:1 or 50:1.

22. The method of claim 16 wherein said depositing said second layer of dielectric is depositing a layer of $Si_3N_4$ using PE-CVD technology at a temperature of about 440 degrees C. said layer to be deposited to a thickens between about 1000 and 2000 Angstrom.

23. The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide ($Al_3O_3$).

24. The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material having a high dielectric constant.

25. The method of claim 16 wherein said etching second layer of dielectric is etching $Si_3N_4$ using $CHF_3$ as etchant gas at a flow rate of about 15 sccm and a gas pressure of about 50 mTorr with an rf power density of about 700 watts with no magnetic field applied and an ambient wafer temperature of about 15 degrees C.

26. The method of claim 16 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said conducting line pattern thereby completing the process of creating a high-aspect ratio pattern of conducting lines said conducting lines being separated with a high dielectric constant Intra-Layer Dielectric.